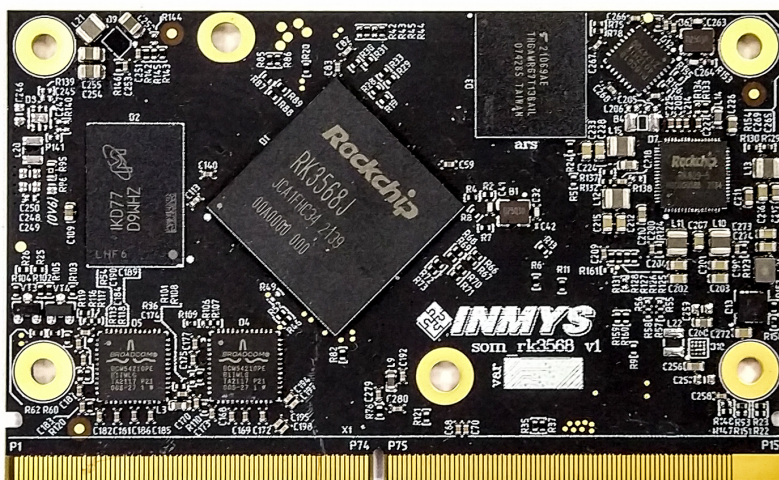


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NMS-SM-RK3568 v1 ds-ru



Процессорный модуль **NMS-SM-RK3568** выполнен на основе процессора производства **Rockchip RK3568**, который оснащен двухъядерным графическим процессором и высокопроизводительным NPU, поддерживающим до 8 ГБ ОЗУ.

Имея различные интерфейсы ввода и вывода видео, он подходит для таких сценариев, как интеллектуальный сетевой видеорегистратор, облачный терминал, шлюз IoT и промышленное управление.

Краткое описание возможностей

Таблица 1: Основные технические характеристики

Внешние разъемы	Краевой разъем в соответствии со SMARC , по стандарту (2.0\2.1)
Процессор	RK3568
	Ядра: 4х-ядерный 64х-битный Cortex-A55, 22нм техпроцесс, частота до 2.0ГГц
	Графический ускоритель: ARM G52 2EE, поддержка OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, Vulkan 1.1
	Видеоускоритель: аппаратное декодирование 4K 60к/с H.265/H.264/VP9, аппаратное кодирование 1080P 100к/с H.265/H.264, 8M ISP, HDR
	Нейросопроцессор: 0.8Tops@INT8, интегрированный высокопроизводительный AI ускоритель RKNN NPU, поддержка Caffe/TensorFlow/TFLite/ONNX/PyTorch/Keras/Darknet
ОЗУ	Память LPDDR4 2 Гбайт (512Mbit x 32) (MT53D512M32D2DS-053WT:D)
Флэш-память	Память eMMC 16 Гбайт (THGAMRG7T13BAIL)
ИС управления питанием	PMIC (RK809-5)
Прочие компоненты	Часы реального времени RTC (PCF8523TK)
	2х Гигабит ETH PHY (BCM54210PEB1IMLG)
	PCIe CLK GEN 25 MHz XTAL→4х 100MHz (PI6CG18401Z)
	Переключатель SATA → USB3 1:2 (CBTL02043A)
Интерфейсы	2х USB 2.0
	1х USB 3.0 OTG
	1х USB 2.0 либо 1х USB 3.0 (USB3_ HOST1_SS замultipлексирован с SATA1)
	1х PCIe 2.1
	2х PCIe 3.0
	2х CAN
	3х UART + 1х отладочный UART
	2х SPI
	3х I2C
	1х I2S
	2х PWM
	1х SATA (замultipлексирован с USB3_ HOST1_SS)
	1х HDMI
	1х eDP
	1х MIPI DSI or LVDS
	1х SDIO
	2х ETH 1GB
	20х GPIO
Напряжение питания	+5 Вольт
Потребление	TBD

Габаритные размеры	82×50 мм
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Файлы для загрузки

Таблица 2: Файлы для загрузки

Название документа	Краткое описание	Версия	Дата
nms-sm-evm_v1_prod_sch.pdf	Схема электрическая принципиальная NMS-SM-EVM v1	v1	2022.09.15
nms-sm-rk3568_v1_prod.step	STEP-файл модуля NMS-SM-RK3568 v1	v1	2022.10.07

Структурная схема модуля

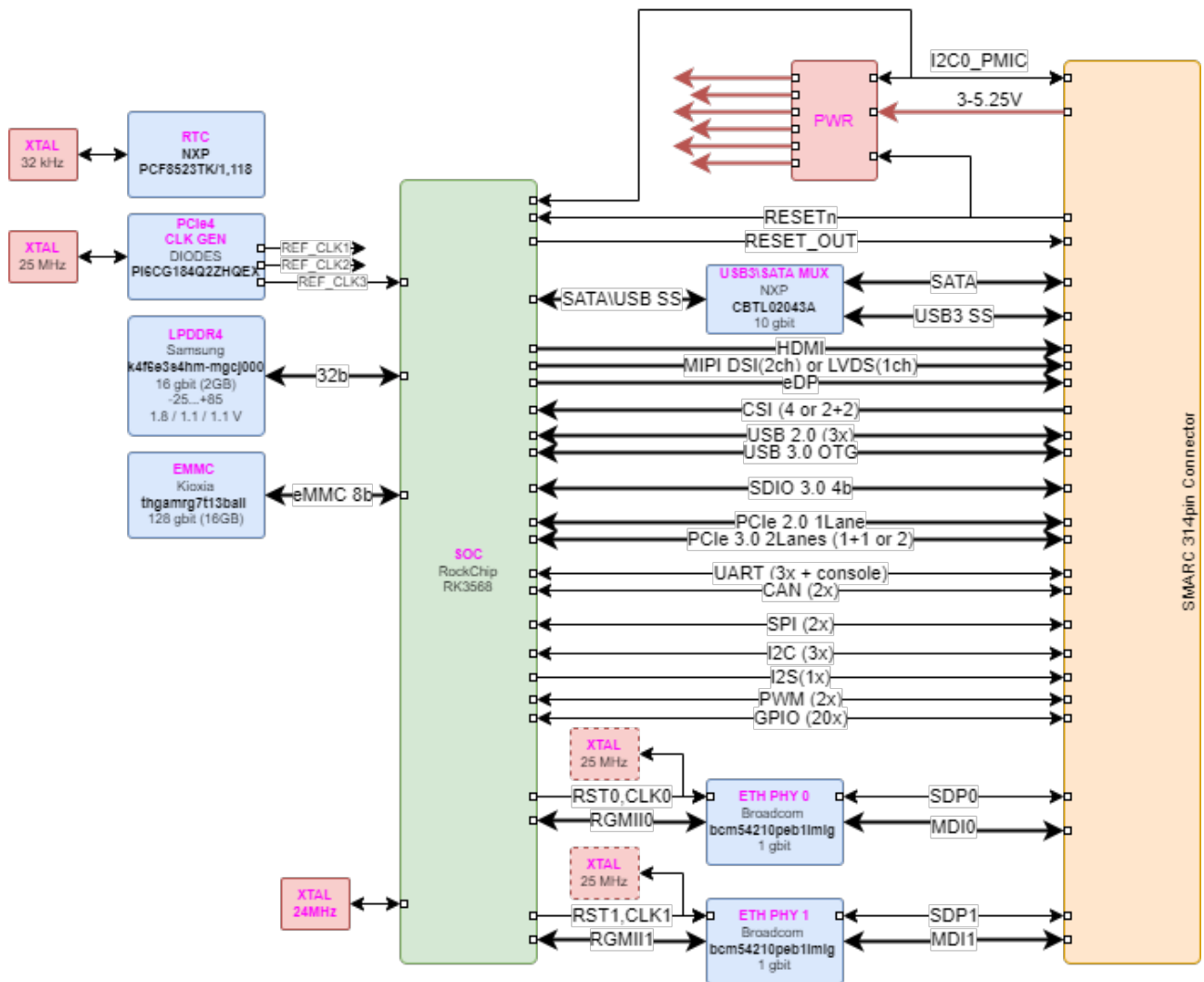


Рисунок 1: Структурная схема модуля

Механические характеристики

Размер платы : 82 x 50 мм.

Печатная плата состоит из 8 слоев, часть из которых являются заземляющими для подавления помех.

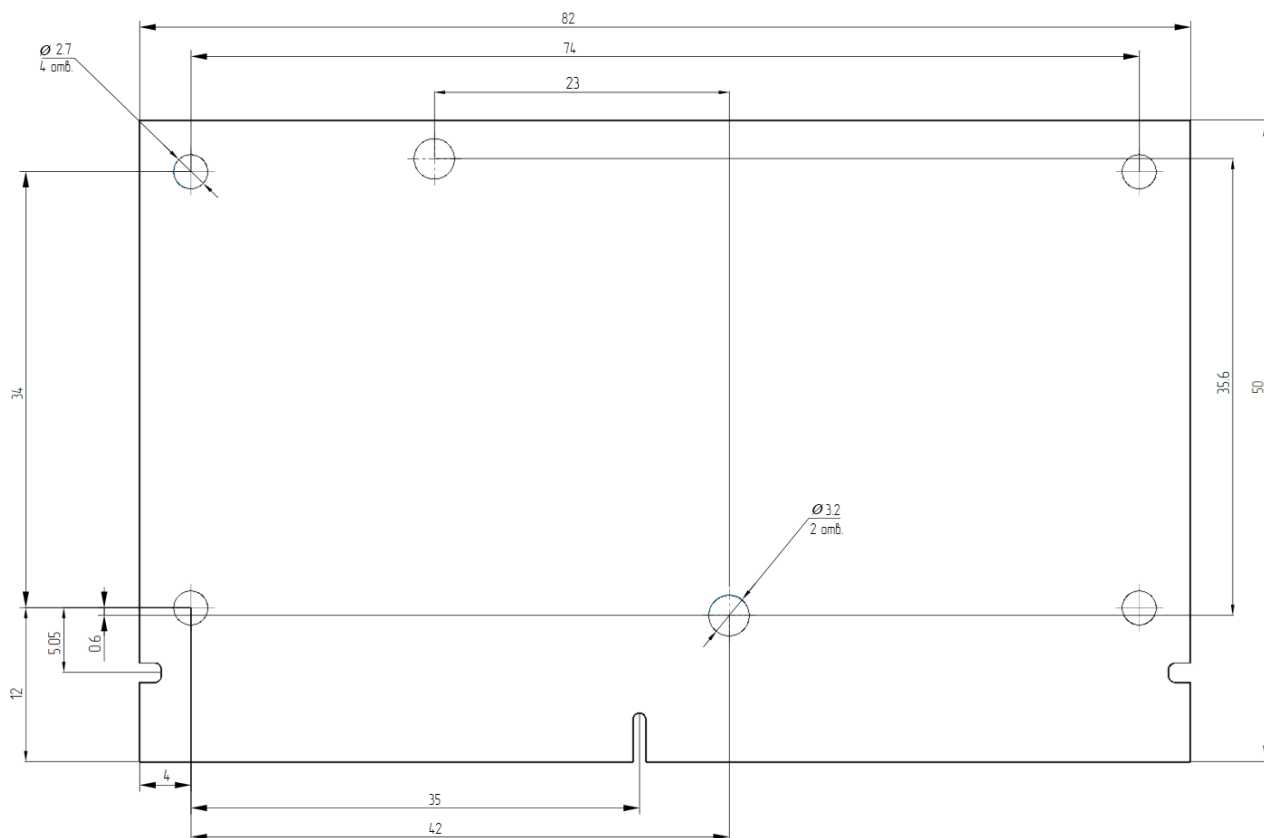


Рисунок 2: Габаритные размеры

Основные аппаратные компоненты

Расположение компонентов на плате

Вид сверху

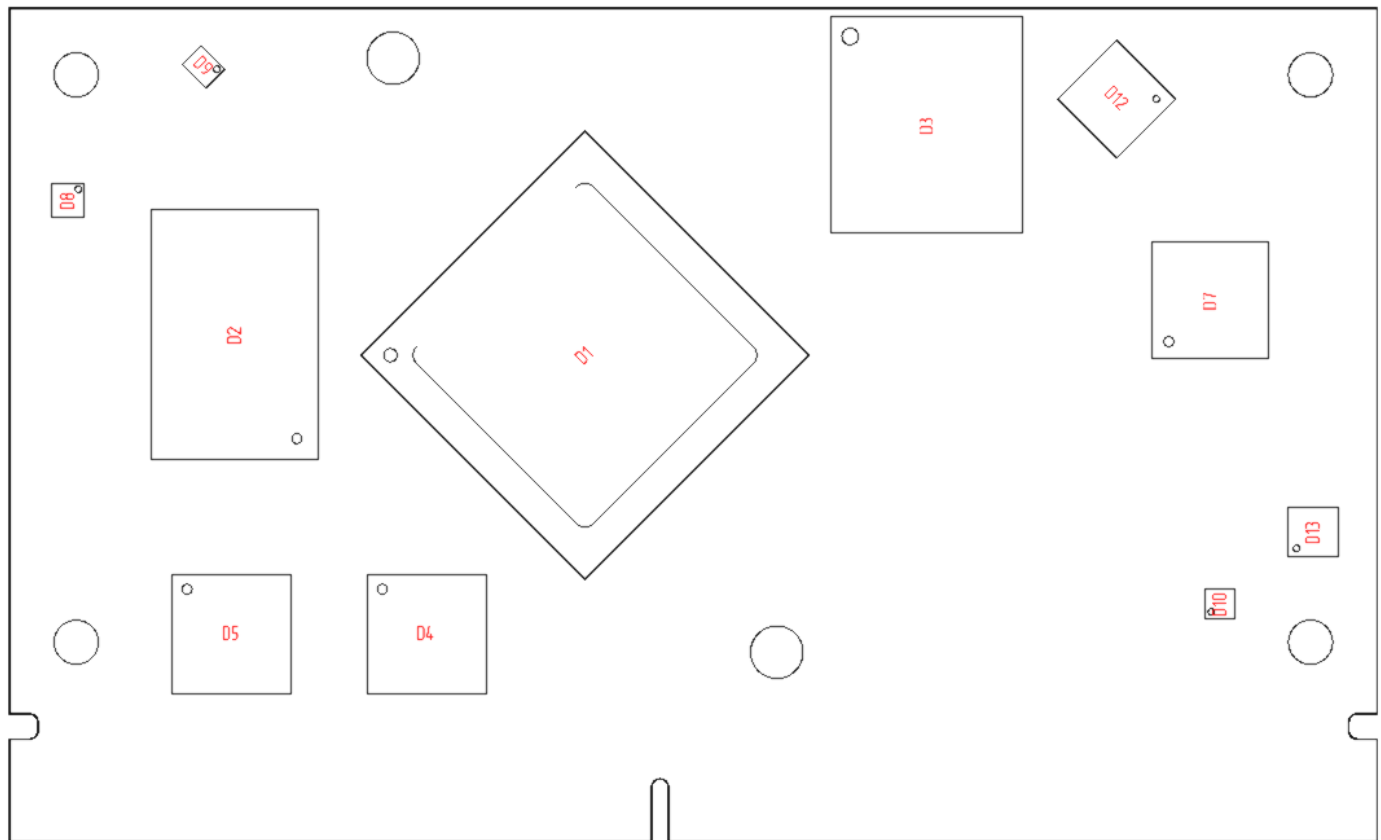


Рисунок 3: Расположение компонентов на плате. Вид сверху

Таблица 3: Наименование компонентов на плате на верхней стороне

Позиционное обозначение	P/N	Описание
D1	RK3568	CPU
D2	MT53D512M32D2DS-053WT:D	LPDDR4
D3	THGAMRG7T13BAIL	EMMC
D4, D5	BCM54210PEB1IMLG	ETH PHY
D7	RK809-5	PMIC
D8	PAM2305CGFADJ	DCDC BUCK
D9	FAN53200UC35X	DCDC BUCK
D10	FAN48623UC50X	DCDC BOOST
D12	PI6CG18401ZHIEX	PCIe CLK GEN
D13	NCP1597BMNTWG	DCDC BUCK

Вид снизу

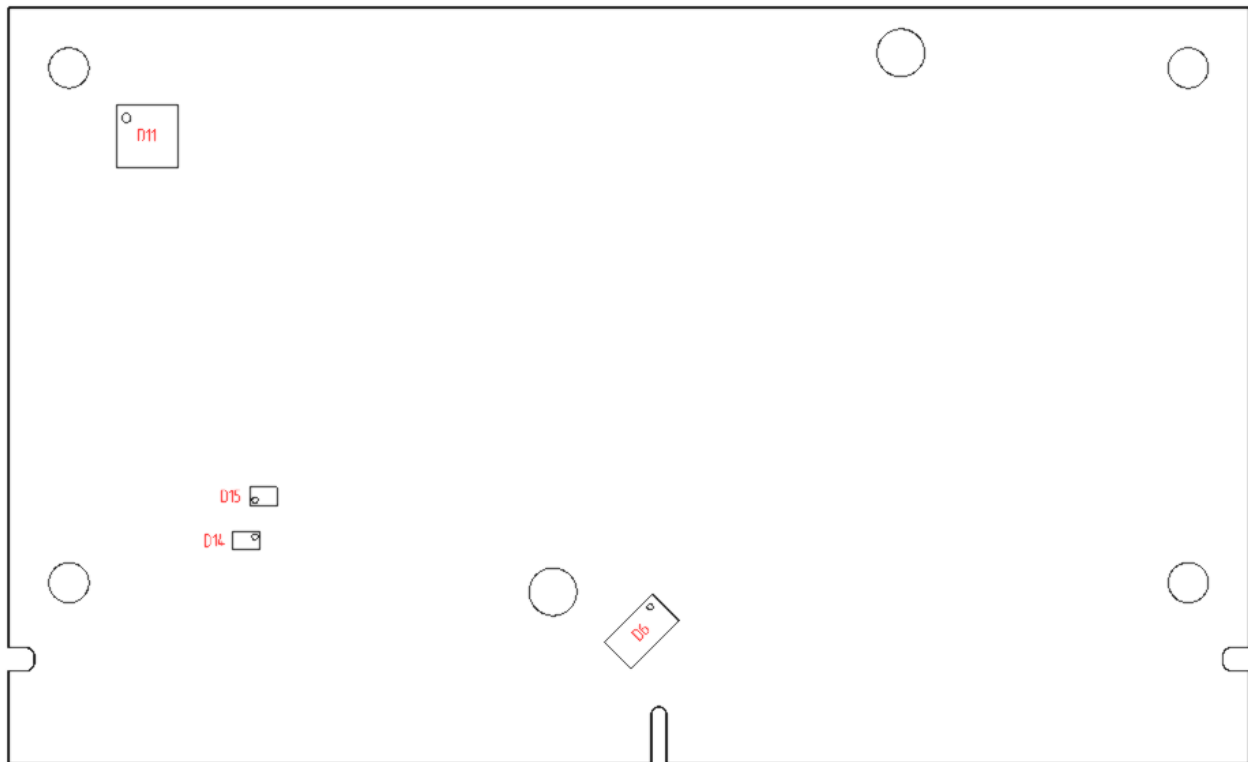


Рисунок 4: Расположение компонентов на плате. Вид снизу

Таблица 4: Наименование компонентов на плате на нижней стороне

Позиционное обозначение	P/N	Описание
D6	CBTL02043ABQ.115	SATA →USB3 1:2 SW
D11	PCF8523TK/1.118	RTC
D14, D15	NLSV2T244MUTAG	LOGIC BUF

Процессор

На рисунке 5 показаны функциональные модули в процессорной системе RK3568.

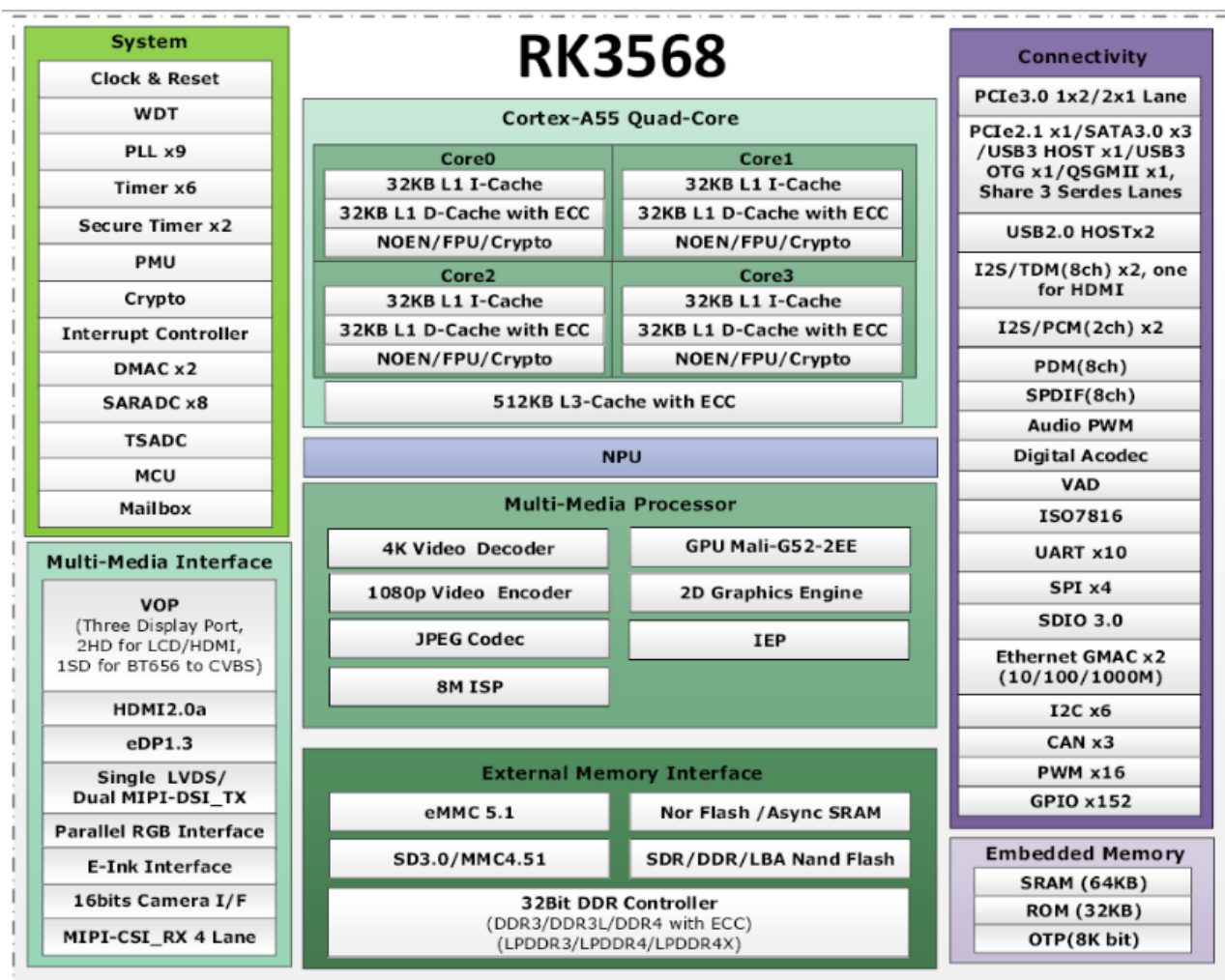
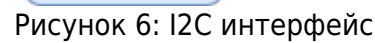


Рисунок 5: Функциональные модули Rockchip RK3568

Интерфейсы

I2C

На плате **NMS-SM-RK3568** доступно три внешних интерфейса I2C и два внутренних для взаимосвязи процессора и периферийных устройств.



Устройство	Адрес
PMIC	0x00110000
DCDC CONV	0x01100000

Устройство	Адрес
RTC	0x01101000
CLK GEN	0x01100001

Расположение разъемов на плате

Вид сверху

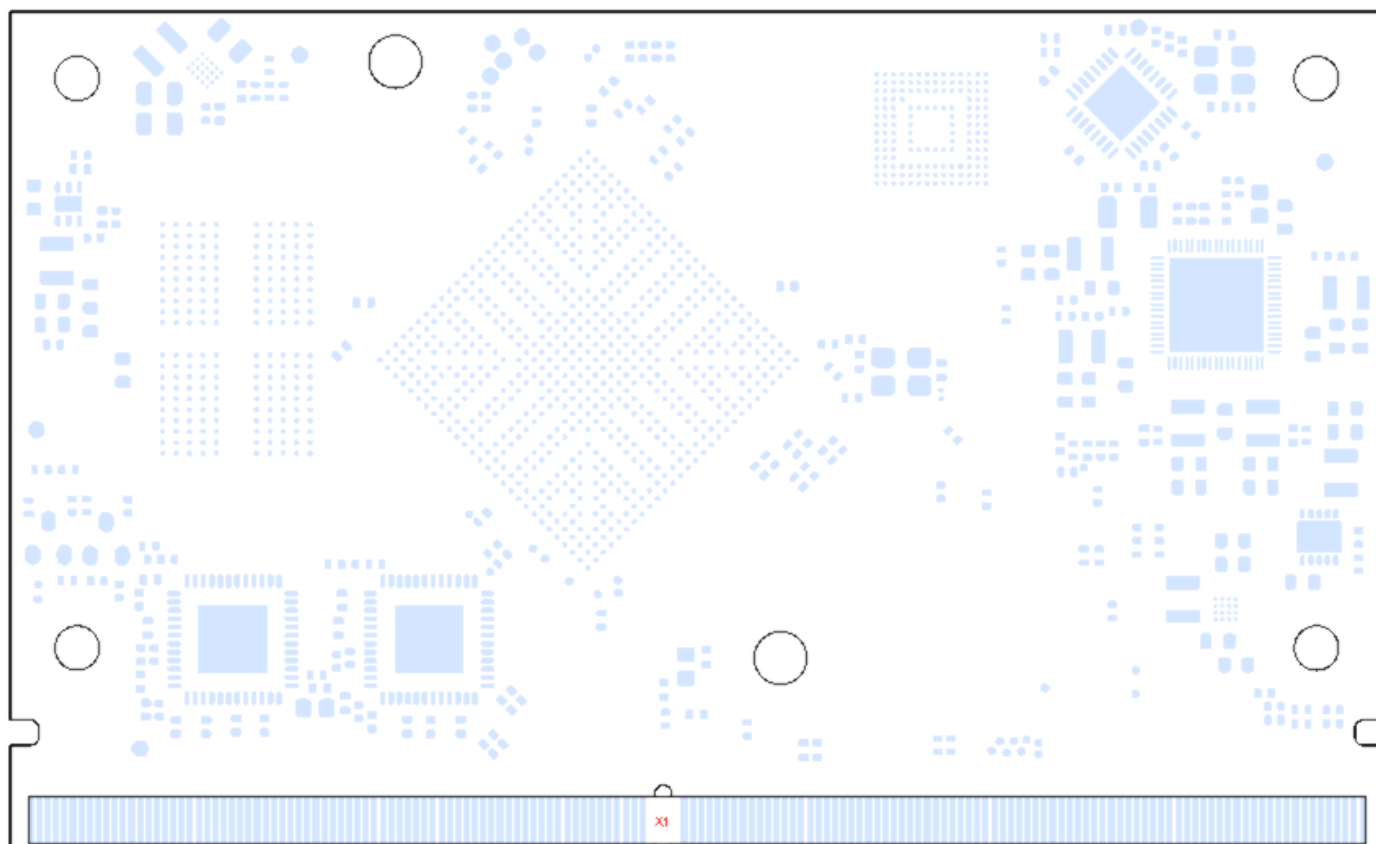


Рисунок 7: Расположение разъемов на плате. Вид сверху

Вид снизу

На нижней стороне платы разъемы отсутствуют.

Распиновка разъемов

Распиновка разъема X1 согласно SMARC

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P1	SMB_ALERT#	NC	-		MANAGEMENT	I OD CMOS	1V8..5V		SMBus Alert# (Interrupt) Signal	Standby/Sleep	
P2	GND	GND			PWR GND						

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5	Group	I/O Type	I/O Level	PV / PD SM_RK3568	Description	Power Domain	Comments
P3	CS1_CK+	MPI_CS1_CLK0_P AG10 MPI_CS1_RX_CLK_OP CS1 I-D-PHY CS1 differential clock input (point to point) Runtime P4 CS1_CK- MPI_CS1_CLK0_N AH10 MPI_CS1_RX_CLK_ON CS1 I-D-PHY CS1 differential clock input (point to point) Runtime P5 GBE1_SDP_ETH1_SDP1_- GBE1 IO_CMOS V3V3 IEEE 1588 Trigger Signal for Hardware Implementation of Precision Time Protocol Standby P6 GBE0_SDP_ETH0_SDP1_- GBE0 IO_CMOS V3V3 IEEE 1588 Trigger Signal for Hardware Implementation of Precision Time Protocol Standby P7 CS1_RX0+ MPI_CS1_D_P AG12 MPI_CS1_RX_D0P CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P8 CS1_RX0- MPI_CS1_D_N AH12 MPI_CS1_RX_D0N CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P9 GND GND PWR_GND P10 CS1_RX1+ MPI_CS1_L_P AG11 MPI_CS1_RX_D1P CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P11 CS1_RX1- MPI_CS1_L_N AH11 MPI_CS1_RX_D1N CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P12 GND GND PWR_GND P13 CS1_RX2+ NC - CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P14 CS1_RX2- NC - CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P15 GND GND PWR_GND P16 CS1_RX3+ NC - CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P17 CS1_RX3- NC - CS1 I-D-PHY /M-PHY CS1 differential input (point to point) Runtime P18 GND GND PWR_GND P19 GBE0_MD1+ ETH0_MD13_N - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P20 GBE0_MD13+ ETH0_MD13_P - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P21 GBE0_LINK100# ETH0_LED_100# - GBE0 IO_OD CMOS V3V3 Link Speed Indication LED for GBE0 100Mbps Standby Shall be able to sink 24mA or more Carrier LED current P22 GBE0_LINK1000# ETH0_LED_1000# - GBE0 IO_OD CMOS V3V3 Link Speed Indication LED for GBE0 1000Mbps Standby Shall be able to sink 24mA or more Carrier LED current P23 GBE0_MD2+ ETH0_MD2_N - GBE0 IO_GBE MD2 Differential Pair Signals for External Transformer Standby P24 GBE0_MD2+ ETH0_MD2_P - GBE0 IO_GBE MD2 Differential Pair Signals for External Transformer Standby P25 GBE0_LINK_ACT# ETH0_LED_ACT# - GBE0 IO_OD CMOS V3V3 Link / Activity Indication LED Driven Low on Link 100 or 1000 Mbps Blinks on Activity Standby Shall be able to sink 24mA or more Carrier LED current P26 GBE0_MD1+ ETH0_MD1_N - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P27 GBE0_MD1+ ETH0_MD1_P - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P28 GBE0_MD1+ ETH0_MD1_P - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P29 GBE0_MD1+ ETH0_MD1_P - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P30 GBE0_MD1+ ETH0_MD1_P - GBE0 IO_GBE MD1 Differential Pair Signals for External Transformer Standby P31 SP10_CS1# SP10_CS1 AD12 MPI_CS1_TX1_DSP SP10 IO_CMOS V1V8 SPI0 Master Chip Select 1 Standby P32 GND GND PWR_GND P33 SDIO_WP SDIO_WP AP25 GPIO0_A5_d SDMMC0_PWREN SATA_AP_SWITCH PCIE20_CLKREQn_M0 SDIO IO_OD CMOS V1V8 or V3V3 PU 10K SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Runtime P34 SDIO_CMD SDMMC0_CMD H27 GPIO2_A1_u SDMMC0_CMD PWM10_M1 UARTS_RX_M0 CAN0_TX_M1 SDIO IO_CMOS V1V8 or V3V3 SDIO CommandResponse. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Runtime P35 SDIO_CD# SDIO_CD# Y22 GPIO0_A4_u SDMMC0_DET SATA_QP_DET PCIE30X1_CLKREQn_M0 SDIO IO_OD CMOS V1V8 or V3V3 PU 10K SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Runtime P36 SDIO_OK SDMMC0_CLK H28 GPIO2_A2_d SDMMC0_CLK TEST_CLKOUT UARTS_TX_M0 CAN0_RX_M1 SDIO IO_CMOS V1V8 or V3V3 SDIO Clock. With every cycle of this signal a one-bit transfer on the command and each data line occurs. Runtime SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its IO voltage level accordingly P37 SDIO_PWR_EN SDIO_PWR_EN AX4 SDIO IO_CMOS V3V3 SDIO Power Enable. This signal is used to enable the power being supplied to a SDMMC card device. Runtime Should be driven low in Standby Mode by the Module P38 GND GND PWR_GND P39 SDIO_DO SDMMC0_DATA2_O J25 SDIO IO_CMOS V1V8 or V3V3 SDIO Data lines. These signals operate in push-pull mode. Runtime P40 SDIO DI SDMMC0_DATA2_I J24 SDIO IO_CMOS V1V8 or V3V3 SDIO Data lines. These signals operate in push-pull mode. Runtime P41 SDIO_D2 SDMMC0_DATA2_I H26 GPIO1_D7_u SDMMC0_D2 AMBITAC_TCK UARTS_CTSn_M0 SDIO IO_CMOS V1V8 or V3V3 SDIO Data lines. These signals operate in push-pull mode. Runtime P42 SDIO_D3 SDMMC0_DATA2_I J23 SDIO IO_CMOS V1V8 or V3V3 SDIO Data lines. These signals operate in push-pull mode. Runtime P43 SDIO Data lines. These signals operate in push-pull mode. Runtime P44 SP10_CS# SP10_CS# IR SP10_CS0_M0 PCIE30X2_PERSTn_M0 SP10 IO_CMOS V1V8 SP10 Master Chip Select 0 Standby This signal can be used to select Carrier SPI as boot device P45 SP10_CS# AC22 GPIO0_B5_u IC22_SCL_M0 SP10_CLK_M0 PCIE20_WAKEn_M0 PWM1_M1 SP10 IO_CMOS V1V8 SP10 Clock Standby P46 SP10_DIN SP10_MISO AC21 GPIO0_C5_d PWMn SP10_MISO_M0 PCIE30X2_WAKEn_M0 SP10 IO_CMOS V1V8 SP10 Master input / Slave output Standby also referred to as MISO P47 SP10_DO SP10_MOSI AA20 GPIO0_B6_u IC22_SDA_M0 SP10_MOSI_M0 PCIE20_PERSTn_M0 PWM2_M1 SP10 IO_CMOS V1V8 SP10 Master output / Slave input Standby also referred to as MOSI P47 GND GND PWR_GND P48 SATA_TX+ SATA1_D_TX_P - SATA O SATA Serial ATA Channel 0 Transmit Output Differential Pair Runtime Series AC coupled on 10 nF Module P49 SATA_TX- SATA1_D_TX_N - SATA O SATA Serial ATA Channel 0 Transmit Output Differential Pair Runtime Series AC coupled on 10 nF Module P50 GND GND PWR_GND P51 SATA_RX+ SATA1_D_RX_P - SATA I Serial ATA Channel 0 Receive Input Differential Pair Runtime Series AC coupled on 10 nF Module P52 SATA_RX- SATA1_D_RX_N - SATA I Serial ATA Channel 0 Receive Input Differential Pair Runtime Series AC coupled on 10 nF Module P53 GND GND PWR_GND P54 ESP1_C50# SP11_C50# OSP1_C50# SP11_C50 AEB GPIO4_C6_d PWM13_M1 SP11_C50_M1 SATA16_ACT_LED UART9_RX_M1 I2S3_SD1_M1 SP11 IO_CMOS V1V8 SP11 Master Chip Select 0 Standby P55 ESP1_C51# SP11_C51# OSP1_C51# SP11_C51 AH6 GPIO4_D1_u HDMITX_CLK_M0 SP11_C51_M1 SP11 IO_CMOS V1V8 SP11 Master Chip Select 1 Standby P56 ESP1_CK SP11_CK OSP1_CK SP11_SCK AR1 GPIO4_C2_d PWM14_M1 SP11_CLK_M1 CAN1_RX_M1 PCIE30X2_CLKREQn_M2 I2S3_MCLK_M1 SP11 IO_CMOS V1V8 SP11 Clock Standby P57 ESP1_IO_1 SP11_DIN OSP1_IO_1 SP11_MISO AD18 GPIO4_C5_d PWM12_M1 SP11_MISO_M1 SATA16_ACT_LED I2S3_SDO_M1 SP11 IO_CMOS V1V8 SP11 Master input / Slave output Standby also referred to as MISO P58 ESP1_IO_0 SP11_DO OSP1_IO_0 SP11_MOSI AA12 GPIO4_C3_d PWM15_R_M1 SP11_MOSI_M1 CAN1_TX_M1 PCIE30X2_WAKEn_M2 I2S3_SCLK_M1	SP11	O CMOS	V1V8	SP11 Master output / Slave input	Standby	also referred to as MOSI			

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Pin #	Name STANDART	Signals_RM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P59	GND	GND	R2	USB2_HOST2_DP	PWR GND	USB0	I/O USB	USB	USB Differential Data Pairs for Port 0	Standby	
P60	USB0+	USB2_HOST2_P	R1	USB2_HOST2_DM	USB0	I/O USB	USB		USB Differential Data Pairs for Port 0	Standby	
P61	USB0-	USB2_HOST2_N		GPIO3_A2_d LCD0_D9 VOP_BT1120_D1 GMAC1_TXD3_M0 I2S3_MCLK_M0 SDMMC2_D1_M1	USB0	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 0	Standby	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P63	USB0_VBUS_DET	NC	-		USB0	USB VBUS 5V	USB VBUS 5V		USB Port 0 Host Power Detection	Standby	
P64	USB0_OTG_ID	NC	-						Input Pin to Announce OTG Device Insertion on USB 2.0 Port	Standby	
P65	USB1+	USB2_HOST3_P	T2	USB2_HOST3_DP	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P66	USB1-	USB2_HOST3_N	T1	USB2_HOST3_DM	USB1	I/O USB	USB		USB Differential Data Pairs for Port 1	Standby	
P67	USB1_EN_OC#	USB2_HOST3_EN_OC#	A64	GPIO3_A3_d LCD0_D10 VOP_BT1120_D2 GMAC1_TXD3_M0 I2S3_SCLK_M0 SDMMC2_D2_M1	USB1	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 1	Standby	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P68	GND	GND			PWR GND						
P69	USB2+	USB3_HOST1_P	P24	USB3_HOST1_DP	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P70	USB2-	USB3_HOST1_N	P25	USB3_HOST1_DM	USB2	I/O USB	USB		USB Differential Data Pairs for Port 2	Standby	
P71	USB2_EN_OC#	USB3_HOST1_EN_OC#	AD2	GPIO3_C0_d LCD0_D23 PWM13_M0 GMAC1_MCLKINOUT_M0 UART3_RX_M1 PDM_SDA0_M2	USB2	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 2	Standby	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P72	RSVD	rsvd	-								
P73	RSVD	rsvd	-								
P74	USB3_EN_OC#	USB3_OTG0_EN_OC#	AH3	GPIO3_A5_d LCD0_D12 VOP_BT1120_D4 GMAC1_RXD3_M0 I2S3_SDO_M0 SDMMC2_CMD_M1	USB3	I/O OD CMOS	3V3	PU 10K	USB Over-Current Sense for Port 3	Standby	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P75	PCIE_A_RST#	PCIE_A_RST#	A88	GPIO3_A1_d LCD0_D8 VOP_BT1120_D0 SPI1_CS0_M1 PCIE30X1_PERSYN_M1 SDMMC2_D0_M1	PCIEA	O CMOS	3V3		PCIE Port A reset output	Runtime	
P76	USB4_EN_OC#	NC	-		USB4	I/O OD CMOS	3V3		USB Over-Current Sense for Port 4	Standby	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
P77	PCIE_B_CKREQ#	PCIE_B_CKREQ#	AF5	GPIO2_D4_d LCD0_D4 VOP_BT656_D4_M0 SPI2_CS1_M1 PCIE30X2_CLKREQ0_M1 I2S1_SDI1_M2	PCIEB	IO OD CMOS	3V3	PU 10K	PCIE Port B clock request	Runtime	
P78	PCIE_A_CKREQ#	PCIE_A_CKREQ#	AC8	GPIO2_D2_d LCD0_D2 VOP_BT656_D2_M0 SPI2_CS0_M1 PCIE30X1_CLKREQ0_M1 I2S1_LRCK_TX_M2	PCIEA	IO OD CMOS	3V3	PU 10K	PCIE Port A clock request	Runtime	
P79	GND	GND			PWR GND						
P80	PCIE_C_REFCK+	PCIE20_REFCLK_P	V24	PCIE20_REFCLK_P	PCIEC	O PCIE			Differential PCIE Link C reference clock output	Runtime	
P81	PCIE_C_REFCK-	PCIE20_REFCLK_N	V25	PCIE20_REFCLK_N	PCIEC	O PCIE			Differential PCIE Link C reference clock output	Runtime	
P82	GND	GND			PWR GND						
P83	PCIE_A_REFCK+	PCIE30_REFCLKA_P	-		PCIEA	O PCIE			Differential PCIE Link A reference clock output	Runtime	
P84	PCIE_A_REFCK-	PCIE30_REFCLKA_N	-		PCIEA	O PCIE			Differential PCIE Link A reference clock output	Runtime	
P85	GND	GND			PWR GND						
P86	PCIE_A_RX+	PCIE30_L0_D_RX_P	AC28	PCIE30_RX0P	PCIEA	I PCIE			Differential PCIE link A receive data pair	Runtime	
P87	PCIE_A_RX-	PCIE30_L0_D_RX_N	AC27	PCIE30_RX0N	PCIEA	I PCIE			Differential PCIE link A receive data pair	Runtime	
P88	GND	GND			PWR GND						
P89	PCIE_A_TX+	PCIE30_L0_D_TX_P	AA28	PCIE30_TX0P	PCIEA	O PCIE			Differential PCIE link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
P90	PCIE_A_TX-	PCIE30_L0_D_TX_N	AA27	PCIE30_TX0N	PCIEA	O PCIE			Differential PCIE link A transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
P91	GND	GND			PWR GND						
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX_D2_P	AG22	HDMI_TX_D2P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX_D2_N	AH22	HDMI_TX_D2N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P94	GND	GND			PWR GND						
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX_D1_P	AG21	HDMI_TX_D1P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX_D1_N	AH21	HDMI_TX_D1N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P97	GND	GND			PWR GND						
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX_D0_P	AG20	HDMI_TX_D0P	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX_D0_N	AH20	HDMI_TX_D0N	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Data Lines	Runtime	
P100	GND	GND			PWR GND						
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX_CLK_P	AH19	HDMI_TX_CLKP	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX_CLK_N	AG19	HDMI_TX_CLKN	HDMI	O TMDS HDMI			HDMI Port, Differential Pair Clock Lines	Runtime	
P103	GND	GND			PWR GND						
P104	HDMI_HPD / DP1_HPD	HDMI_HPD	AB18	HDMI_TX_HPDIN	HDMI	I CMOS	1V8	PD 1M	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	Runtime	
P105	HDMI_CTRL_CLK / DP1_AUX+	HDMI_CTRL_SCL	AG68	GPIO4_C7_d HDMITX_SCL I2CS_SCL_M1	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_CLK Line Dedicated to HDMI	Runtime	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_CTRL_SDA	AG67	GPIO4_D0_u HDMITX_SDA I2CS_SDA_M1	HDMI	I/O OD CMOS	1V8	PU 100K	I2C_DAT Line Dedicated to HDMI	Runtime	
P107	DP1_AUX_SEL	NC	-		DP1++_HDMI	I CMOS	1V8		Strapping Signal to Enable Either HDMI or DP Output	Runtime	0 - DP 1 - HDMI
P108	GPIO0 / CAM0_PWR#	GPIO.0	AA5	GPIO3_D5_d CF_D7 EBC_SDD07 SDMMC2_PWREN_M0 I2S1_SDI0_M1 VOP_BT656_D7_M1	GPIO	IO CMOS	1V8		GPIO Pin 0 Preferred Output	Runtime	Shared with CAM0_PWR#
P109	GPIO1 / CAM1_PWR#	GPIO.1	AC1	GPIO3_D3_d CF_D5 EBC_SDD05 SDMMC2_CLK_M0 I2S1_SDI1_M1 VOP_BT656_D5_M1	GPIO	IO CMOS	1V8		GPIO Pin 1 Preferred Output	Runtime	Shared with CAM1_PWR#
P110	GPIO2 / CAM0_RST#	GPIO.2	AA1	GPIO3_D4_d CF_D6 EBC_SDD06 SDMMC2_DET_M0 I2S1_SDI2_M1 VOP_BT656_D6_M1	GPIO	IO CMOS	1V8		GPIO Pin 2 Preferred Output	Runtime	Shared with CAM0_RST#
P111	GPIO3 / CAM1_RST#	GPIO.3	Y7	GPIO3_D2_d CF_D4 EBC_SDD04 SDMMC2_CMD_M0 I2S1_SDI0_M1 VOP_BT656_D4_M1	GPIO	IO CMOS	1V8		GPIO Pin 3 Preferred Output	Runtime	Shared with CAM1_RST#
P112	GPIO4 / HDA_RST#	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 4 Preferred Output	Runtime	Shared with HDA_RST#
P113	GPIO5 / PWM_OUT	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 5 Preferred Output	Runtime	Shared with PWM_OUT
P114	GPIO6 / TACHIN	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 6 Preferred Output	Runtime	Shared with TACHIN
P115	GPIO7	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 7 Preferred Output	Runtime	
P116	GPIO8	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 8 Preferred Output	Runtime	
P117	GPIO9	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 9 Preferred Output	Runtime	
P118	GPIO10	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 10 Preferred Output	Runtime	
P119	GPIO11	NC	-		GPIO	IO CMOS	1V8		GPIO Pin 11 Preferred Output	Runtime	
P120	GND	GND			PWR GND						
P121	I2C_PM_CLK	I2C_PM_SCL	AF24	GPIO0_B1_u I2C0_SCL	MANAGEMENT	IO OD CMOS	1V8	PU 2K2	Power management I2C bus CLK	Standby/Sleep	
P122	I2C_PM_DAT	I2C_PM_SDA	AB21	GPIO0_B2_u I2C0_SDA	MANAGEMENT	IO OD CMOS	1V8	PU 2K2	Power management I2C bus DATA	Standby/Sleep	
P123	BOOT_SEL0#	BOOT.0	A24	GPIO1_B4_u EMMC_D0 FLASH_D0	BOOT	I OD CMOS	1V8	PU 10K	Input straps determine the Module boot device.	Standby	
P124	BOOT_SEL1#	NC	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P125	BOOT_SEL2#	NC	-		BOOT	I OD CMOS	1V8		Input straps determine the Module boot device.	Standby	
P126	RESET_OUT#	RESET_OUT#	AC24	GPIO0_D6_d	MANAGEMENT	O CMOS	1V8		General purpose reset output to Carrier Board.	Standby	
P127	RESET_IN#	RESET_IN#	AH27	HPOR_u	MANAGEMENT	I OD CMOS	1V8..5V	PU 10K	Reset input from Carrier Board. Carrier drives low to force a Module reset, floats the line otherwise. This signal shall be level triggered during bootup to allow to stop booting of the module. After bootup it may act as an edge triggered signal.	Standby	
P128	POWER_BTN#	POWER_BTN#	-		MANAGEMENT	I OD CMOS	1V8..5V	PU 10K	Power-button input from Carrier Board. Carrier to float the line in inactive state. Active low, level sensitive. Should be debounced on the Module.	Sleep	
P129	SER0_TX	SER0.RXTX.TX	F26	GPIO2_C5_d I2S2_SDI_M0 GMAC0_RXER UART8_TX_M0 SPI2_CS1_M0	SER0	O CMOS	1V8		Asynchronous Serial Data Output Port 0	Runtime	
P130	SER0_RX	SER0.RXTX.RX	E26	GPIO2_C6_d CLK32K_OUT1 UART8_RX_M0 SPI1_CS1_M0	SER0	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 0	Runtime	
P131	SER0_RTS#	SER0.RTS	D26	GPIO2_B1_d SDMMC1_PWREN I2C4_SDA_M1 UART8_RTSn_M0 CAN2_RX_M1	SER0	O CMOS	1V8		Request to Send Handshake Line for Port 0	Runtime	
P132	SER0_CTS#	SER0.CTS	E25	GPIO2_B2_u SDMMC1_DET I2C4_SCL_M1 UART8_CTSn_M0 CAN2_TX_M1	SER0	I CMOS	1V8	PU 100K	Clear to Send Handshake Line for Port 0	Runtime	

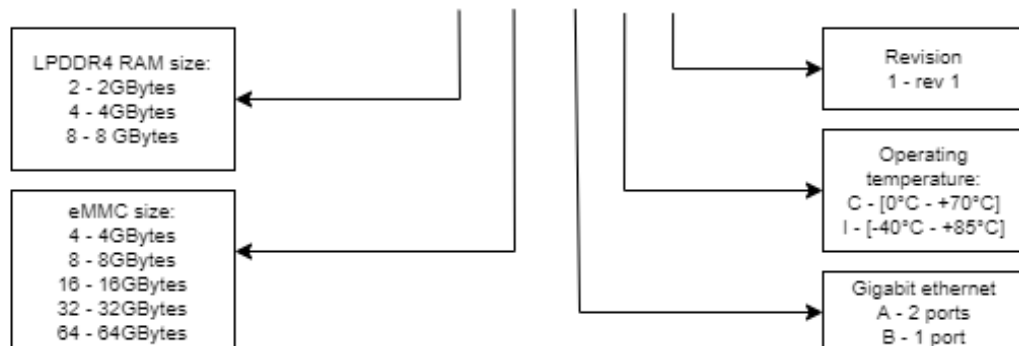
Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
P133	GND	GND				PWR GND					
P134	SER1_TX	SER1.TX	AH24	GPIO0_D1_u UART2_TX_M0	SER1	O CMOS	1V8		Asynchronous Serial Data Output Port 1	Runtime	
P135	SER1_RX	SER1.RX	AC20	GPIO0_D0_u UART2_RX_M0	SER1	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 1	Runtime	
P136	SER2_TX	SER2.RXTX.TX	AF2	GPIO3_B2_d LCD_C_D17 VOP_BT1120_D8 GMAC1_RXD0_M0 UART4_TX_M1 PWM9_M0	SER2	O CMOS	1V8		Asynchronous Serial Data Output Port 2	Runtime	
P137	SER2_RX	SER2.RXTX.RX	AG1	GPIO3_D1_d LCD_C_D16 VOP_BT1120_D7 GMAC1_RXD0_M0 UART4_RX_M1 PWM9_M0	SER2	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 2	Runtime	
P138	SER2_RTS#	NC	-		SER2	O CMOS	1V8		Request to Send Handshake Line for Port 2	Runtime	
P139	SER2_CTS#	NC	-		SER2	I CMOS	1V8		Clear to Send Handshake Line for Port 2	Runtime	
P140	SER3_TX	SER3.TX	AA7	GPIO3_C2_d LCD_C_VSYNC VOP_BT1120_D14 SPI1_MISO_M1 UART5_TX_M1 I2S1_SDO3_M2	SER3	O CMOS	1V8		Asynchronous Serial Data Output Port 3	Runtime	
P141	SER3_RX	SER3.RX	AC4	GPIO3_C3_d LCD_C_DEIN VOP_BT1120_D15 SPI1_CLK_M1 UART5_RX_M1 I2S1_SCLK_RX_M1	SER3	I CMOS	1V8	PU 100K	Asynchronous Serial Data Input Port 3	Runtime	
P142	GND	GND				PWR GND					
P143	CAN0_TX	CAN0.TX	AG24	GPIO0_B3_u I2C1_SCL CAN0_TX_M0 POIE30X1_BUTTONRSTn MCU_JTAG_TDO	CAN0	O CMOS	1V8		CAN Port 0 Transmit Output	Runtime	
P144	CAN0_RX	CAN0.RX	AB20	GPIO0_B4_u I2C1_SDA CAN0_RX_M0 POIE20_BUTTONRSTn MCU_JTAG_TCK	CAN0	I CMOS	1V8		CAN Port 0 Receive Input	Runtime	
P145	CAN1_TX	CAN1.TX	V5	GPIO4_B5_d I2C2_SCL_M1 EBC_SDSIR CAN2_TX_M0 I2S1_SDO3_M1	CAN1	O CMOS	1V8		CAN Port 1 Transmit Output	Runtime	
P146	CAN1_RX	CAN1.RX	V6	GPIO4_B4_d I2C2_SDA_M1 EBC_QDSP CAN2_RX_M0 ISP_FLASH_TRIGIN VOP_BT656_CLK_M1	CAN1	I CMOS	1V8		CAN Port1 Receive Input	Runtime	
P147	VDD_IN	VDD_IN				PWR	3V..5.25V				
P148	VDD_IN	VDD_IN				PWR	3V..5.25V				
P149	VDD_IN	VDD_IN				PWR	3V..5.25V				
P150	VDD_IN	VDD_IN				PWR	3V..5.25V				
P151	VDD_IN	VDD_IN				PWR	3V..5.25V				
P152	VDD_IN	VDD_IN				PWR	3V..5.25V				
P153	VDD_IN	VDD_IN				PWR	3V..5.25V				
P154	VDD_IN	VDD_IN				PWR	3V..5.25V				
P155	VDD_IN	VDD_IN				PWR	3V..5.25V				
P156	VDD_IN	VDD_IN				PWR	3V..5.25V				
51	CSI1_TX+ / I2C_CAM1_CK	NC	-		CSI1	I/O OD CMOS	1V8		I2C clock for serial camera data support link or differential data lane	Runtime	CSI2_0
52	CSI1_TX- / I2C_CAM1_DAT	NC	-		CSI1	I/O OD CMOS	1V8		I2C data for serial camera data support link or differential data lane	Runtime	CSI2_0
53	GND	GND	-			PWR GND					
54	RSTVD	rstvd	-			PWR GND					
55	CSI0_TX+ / I2C_CAM0_CK	I2C_CAM0_SCL	V1	GPIO4_B3_d I2C4_SCL_M0 EBC_GDDE ETH1_REFCLK0_25M_M1 SPI3_CLK_M0 I2S2_SDO_M1	CSI0	I/O OD CMOS	1V8	PU 2K2	I2C clock for serial camera data support link or differential data lane	Runtime	CSI2_0
56	CAM_MCK	CAM_MCK	U3	GPIO4_C0_d C_F_CLKOUT EBC_GDCLK PWM11_IR_M1	CSI	O CMOS	1V8		Master clock output	Runtime	
57	CSI0_TX- / I2C_CAM0_DAT	I2C_CAM0_SDA	V4	GPIO4_B2_d I2C4_SDA_M0 EBC_VCOM GMAC1_RXER_M1 SPI3_MOSI_M0 I2S2_SDI_M1	CSI0	I/O OD CMOS	1V8	PU 2K2	I2C data for serial camera data support link or differential data lane	Runtime	CSI2_0
58	CSI0_CK+	MIPI_CSI_CLK1_P	AG9	MIPI_CSI_RX_CLK3P	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
59	CSI0_CK-	MIPI_CSI_CLK1_N	AH9	MIPI_CSI_RX_CLK1N	CSI0	I D-PHY			CSI0 differential clock input (point to point)	Runtime	
510	GND	GND				PWR GND					
511	CSI0_RX0+	MIPI_CSI_2_P	AE11	MIPI_CSI_RX_D2P	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
512	CSI0_RX0-	MIPI_CSI_2_N	AD11	MIPI_CSI_RX_D2N	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
513	GND	GND				PWR GND					
514	CSI0_RX1+	MIPI_CSI_3_P	AD9	MIPI_CSI_RX_D3P	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
515	CSI0_RX1-	MIPI_CSI_3_N	AE9	MIPI_CSI_RX_D3N	CSI0	I D-PHY / I M-PHY			CSI0 differential input	Runtime	
516	GND	GND				PWR GND					
517	GBE1_MDIO+	ETH1_MDIO_P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
518	GBE1_MDIO-	ETH1_MDIO_N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
519	GBE1_LINK100#	ETH1_LED_100#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 100Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
520	GBE1_MDIO+	ETH1_MDIO1_P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
521	GBE1_MDIO-	ETH1_MDIO1_N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
522	GBE1_LINK1000#	ETH1_LED_1000#	-		GBE1	O OD CMOS	3V3		Link Speed Indication LED for GBE1 1000Mbps	Standby	Shall be able to sink 24mA or more Carrier LED current.
523	GBE1_MDIO2+	ETH1_MDIO2_P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
524	GBE1_MDIO2-	ETH1_MDIO2_N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
525	GND	GND				PWR GND					
526	GBE1_MDIO3+	ETH1_MDIO3_P	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
527	GBE1_MDIO3-	ETH1_MDIO3_N	-		GBE1	I/O GBE MDI			Differential Pair Signals for External Transformer	Standby	
528	GBE1_CTREF	NC	-		GBE1	Analog	0...3V3		Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic (if required by the Module GBE PHY)	Standby	
529	PCIE_D_TX+ / SERDES_0_TX+	NC	-		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
530	PCIE_D_TX- / SERDES_0_TX-	NC	-		PCIED	O PCIE			Differential PCIe link D transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIe generation
531	GBE1_LINK_ACT#	ETH1_LED_ACT#	-		GBE1	O OD CMOS	3V3		Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	Standby	Shall be able to sink 24mA or more Carrier LED current.
532	PCIE_D_RX+ / SERDES_0_RX+	NC	-		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
533	PCIE_D_RX- / SERDES_0_RX-	NC	-		PCIED	I PCIE			Differential PCIe link D receive data pair	Runtime	
534	GND	GND				PWR GND					
535	USB4+	NC	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
536	USB4-	NC	-		USB4	I/O USB	USB		USB Differential Data Pairs for Port 4	Standby	
537	USB3_VBUS_DET	USB3_VBUS_DET	M24	USB3_OTG0_VBUSDET	USB3	USB VBUS 5V	USB VBUS 5V		USB Port 3 Host Power Detection	Standby	
538	AUDIO_MCK	AUDIO_MCK	A19	GPIO1_A2_d I2S1_MCLK_M0 UART3_RTSn_M0 SCR_CLK POIE30X1_PERSn_M2	I2S	O CMOS	1V8		Master Clock Output to I2S Codec(s)	Runtime	
539	I2S0_LRCK	I2S0.FS	A20	GPIO1_A3_d I2S1_LRCK_TX_M0 UART4_RTSn_M0 SCR_RST POIE30X1_CLKREQn_M2 ACODEC_DAC_SYNC	I2S0	I/O CMOS	1V8		I2S0 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
540	I2S0_SDOUT	I2S0.DOUT	B20	GPIO1_A7_d I2S1_SDO0_M0 UART4_CTSn_M0 SCR_DET AUDIOPWM_ROUT_N ACODEC_DAC_DATA1	I2S0	O CMOS	1V8		I2S0 Digital Audio Output	Runtime	
541	I2S0_SDIN	I2S0.DIN	B21	GPIO1_B3_d I2S1_SDI0_M0 PDM_SDI0_M0	I2S0	I CMOS	1V8		I2S0 Digital Audio Input	Runtime	
542	I2S0_CK	I2S0.SCLK	B19	GPIO1_A3_d I2S1_SCLK_TX_M0 UART3_CTSn_M0 SCR_IO POIE30X1_WAKEN_M2 ACODEC_DAC_CLK	I2S0	I/O CMOS	1V8		I2S0 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
543	ESPI_ALERT0#	NC	-		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	
544	ESPI_ALERT1#	NC	-		eSPI	I OD CMOS	1V8		ESPI ALERT	Standby	
545	MDIO_CLK	NC	-		SERDES	O CMOS	1V8		MDIO Signals to Configure Possible PHYs		
546	MDIO_DAT	NC	-		SERDES	I/O OD CMOS	1V8		MDIO Signals to Configure Possible PHYs		
547	GND	GND				PWR GND					
548	I2C_GP_CK	I2C_GP_SCL	E18	GPIO1_A1_u I2C3_SCL_M0 UART3_TX_M0 CAN1_TX_M0 AUDIOPWM_LOUT_N ACODEC_ADC_CLK	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Clock Signal	Runtime	
549	I2C_GP_DAT	I2C_GP_SDA	D18	GPIO1_A0_u I2C3_SDA_M0 UART3_RX_M0 CAN1_RX_M0 AUDIOPWM_LOUT_P ACODEC_ADC_DATA	I2C_GP	I/O OD CMOS	1V8	PU 2K2	General Purpose I2C Data Signal	Runtime	

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S50	HDA_SYNC / I2S2_LRCK	NC	-		I2S2	I/O CMOS	1V8		I2S2 Left & Right Synchronization Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S51	HDA_SDO / I2S2_SDOOUT	NC	-		I2S0	O CMOS	1V8		I2S2 Digital Audio Output	Runtime	
S52	HDA_SDI / I2S2_SDOIN	NC	-		I2S0	I CMOS	1V8		I2S2 Digital Audio Input	Runtime	
S53	HDA_CK / I2S2_CK	NC	-		I2S0	I/O CMOS	1V8		I2S2 Digital Audio Clock	Runtime	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
S54	SATA_ACT#	NC	-		SATA	O OD CMOS	3V3		SATA Activity Indicator	Runtime	Pulled low by Module OD driver to disable USB5 power. Pulled low by Carrier OD driver to indicate overcurrent situation.
S55	USB5_EN_OC#	NC	-		USB5	I/O OD CMOS	3V3		USB Over-Current Sense for Port 5	Standby	
S56	ESPI_IO_2 / OSPI_IO_2	NC	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S57	ESPI_IO_3 / OSPI_IO_3	NC	-		QSPI	I/O CMOS	1V8		QSPI Data input / output	Standby	
S58	ESPI_RESET#	NC	-		eSPI	O CMOS	1V8		ESPI Reset	Standby	
S59	USB5+	NC	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S60	USB5-	NC	-		USB5	I/O USB	USB		USB Differential Data Pairs for Port 5	Standby	
S61	GND		-		PWR GND						
S62	USB3_SSTX+	USB3_OTG0_SS_D_TX_P	T28	USB3_OTG0_SSTXP SATA0_TXP	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S63	USB3_SSTX-	USB3_OTG0_SS_D_TX_N	T27	USB3_OTG0_SSTXN SATA0_TXN	USB3	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 3	Standby	DC blocking capacitors 100nF shall be placed on the Module
S64	GND		-		PWR GND						
S65	USB3_SSRX+	USB3_OTG0_SS_D_RX_P	R28	USB3_OTG0_SSRXP SATA0_RXP	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S66	USB3_SSRX-	USB3_OTG0_SS_D_RX_N	R27	USB3_OTG0_SSRXN SATA0_RXN	USB3	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 3	Standby	
S67	GND		-		PWR GND						
S68	USB3+	USB3_OTG0_DP	P27	USB3_OTG0_DP	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S69	USB3-	USB3_OTG0_DN	P28	USB3_OTG0_DN	USB3	I/O USB	USB		USB Differential Data Pairs for Port 3	Standby	
S70	GND		-		PWR GND						
S71	USB2_SSTX+	USB3_HOST1_SS_D_TX_P	V28	USB3_HOST1_SSTXP SATA1_TXP	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S72	USB2_SSTX-	USB3_HOST1_SS_D_TX_N	V27	USB3_HOST1_SSTXN SATA1_TXN	USB2	O USB SS	USB SS		Transmit Signal Differential Pairs for SuperSpeed on Port 2	Standby	DC blocking capacitors 100nF shall be placed on the Module
S73	GND		-		PWR GND						
S74	USB2_SSRX+	USB3_HOST1_SS_D_RX_P	U28	USB3_HOST1_SSRXP SATA1_RXP	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S75	USB2_SSRX-	USB3_HOST1_SS_D_RX_N	U27	USB3_HOST1_SSRXN SATA1_RXN	USB2	I USB SS	USB SS		Receive Signal Differential Pairs for SuperSpeed on Port 2	Standby	
S76	PCIE_B_RST#	PCIE_B_RST#	AD6	GPIO2_D6_d LCDC_D6 VOP_BT656_D6_M0 SPI2_MOSI_M1 PCIE002_PERRStn_M1 I2S1_SDI3_M2 GPIO3_C1_d LCDC_JSTYN VOP_BT1120_D13 SPI1_MOSI_M1 PCIE20_PERRStn_M1 I2S1_SDO2_M2	PCIEB	O CMOS	3V3		PCIE Port B reset output	Runtime	
S77	PCIE_C_RST#	PCIE_C_RST#	AD1	GPIO3_C1_d LCDC_JSTYN VOP_BT1120_D13 SPI1_MOSI_M1 PCIE20_PERRStn_M1 I2S1_SDO2_M2	PCIEC	O CMOS	3V3		PCIE Port C reset output	Runtime	
S78	PCIE_C_RX+ / SERDES_3_RX+	PCIE20_D_RX_P	Y27	PCIE20_RXP SATA2_RXP	PCIEC	I PCIE			Differential PCIE link C receive data pair	Runtime	
S79	PCIE_C_RX- / SERDES_3_RX-	PCIE20_D_RX_N	Y28	PCIE20_RXN SATA2_RXN	PCIEC	I PCIE			Differential PCIE link C receive data pair	Runtime	
S80	GND		-		PWR GND						
S81	PCIE_C_TX+ / SERDES_1_TX+	PCIE20_D_TX_P	W27	PCIE20_TXP SATA2_TXP	PCIEC	O PCIE			Differential PCIE link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
S82	PCIE_C_TX- / SERDES_1_TX-	PCIE20_D_TX_N	W28	PCIE20_TXN SATA2_TXN	PCIEC	O PCIE			Differential PCIE link C transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
S83	GND		-		PWR GND						
S84	PCIE_B_REFCK+	PCIE30_REFCLKB_P	-	PCIEB	O PCIE				Differential PCIE link B reference clock output	Runtime	
S85	PCIE_B_REFCK-	PCIE30_REFCLKB_N	-	PCIEB	O PCIE				Differential PCIE link B reference clock output	Runtime	
S86	GND		-		PWR GND						
S87	PCIE_B_RX+	PCIE30_L1_D_RX_P	AD28	PCIE30_RX1P	PCIEB	I PCIE			Differential PCIE link B receive data pair	Runtime	
S88	PCIE_B_RX-	PCIE30_L1_D_RX_N	AD27	PCIE30_RX1N	PCIEB	I PCIE			Differential PCIE link B receive data pair	Runtime	
S89	GND		-		PWR GND						
S90	PCIE_B_TX+	PCIE30_L1_D_TX_P	AB28	PCIE30_TX1P	PCIEB	O PCIE			Differential PCIE link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
S91	PCIE_B_TX-	PCIE30_L1_D_TX_N	AB27	PCIE30_TX1N	PCIEB	O PCIE			Differential PCIE link B transmit data pair	Runtime	Series AC coupled on Module 75-265 nF depending on PCIE generation
S92	GND		-		PWR GND						
S93	DP0_LANE0+	EDP_TX_D0_P	J28	EDP_TX_D0P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S94	DP0_LANE0-	EDP_TX_D0_N	K27	EDP_TX_D0N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S95	DP0_AUX_SEL	NC	-		DP0++	I CMOS	1V8		Auxiliary Selection	Runtime	
S96	DP0_LANE1+	EDP_TX_D1_P	K28	EDP_TX_D1P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S97	DP0_LANE1-	EDP_TX_D1_N	L27	EDP_TX_D1N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S98	DP0_HPD	DP0_HPD	AG23	GPIO0_C2_d PWM3_IR EDP_HPDIN_M1 PCIE001_WAKEStn_M0 MCU_JTAG_TMS	DP0++	I CMOS	1V8	PD 1M	DP Hot Plug Detect Input	Runtime	
S99	DP0_LANE2+	EDP_TX_D2_P	L28	EDP_TX_D2P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S100	DP0_LANE2-	EDP_TX_D2_N	M27	EDP_TX_D2N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S101	GND		-		PWR GND						
S102	DP0_LANE3+	EDP_TX_D3_P	M28	EDP_TX_D3P	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S103	DP0_LANE3-	EDP_TX_D3_N	N27	EDP_TX_D3N	DP0++	O DP			Primary DP Port Differential Pair Data Lines	Runtime	
S104	USB3_OTG_ID	USB3_OTG0_ID	L23	USB3_OTG0_ID	USB3	I CMOS	3V3		Input Pin to Announce OTG Device Insertion on USB 3.2 Port	Standby	
S105	DP0_AUX+	EDP_TX_AUX_P	L25	EDP_TX_AUXP	DP0++	I/O DP	3V3	PD 100K	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module, if DP0_AUX_SEL=1 (HDMI) - DC coupled
S106	DP0_AUX-	EDP_TX_AUX_N	M25	EDP_TX_AUXN	DP0++	I/O DP	3V3	PU 100K	Primary DP Port Bidirectional Channel used for Link Management and Device Control	Runtime	AC coupled on module, if DP0_AUX_SEL=1 (HDMI) - DC coupled
S107	LCD1_BKLT_EN	LCD1_BKLT_EN	AF23	GPIO0_C1_d PWM2_M0 NPUVTS UART0_TX MCU_JTAG_TDI	eDP1	O CMOS	1V8		Secondary LVDS Channel Backlight Enable	Runtime	
S108	LVDS1_CK+ / eDP0_AUX+ / DS10_CLK+	MIP1_DSI_TX1.4_P	AD15	MIP1_DSI_TX1_CLKP	DS10	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S109	LVDS1_CK- / eDP0_AUX- / DS10_CLK-	MIP1_DSI_TX1.4_N	AE15	MIP1_DSI_TX1_CLKN	DS10	O D-PHY			Secondary DSI Panel Differential Pair Clock Lines	Runtime	
S110	GND		-		PWR GND						
S111	LVDS1_0+ / eDP0_TX0+ / DS10_D0+	MIP1_DSI_TX1.0_P	AD18	MIP1_DSI_TX1_D0P	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S112	LVDS1_0- / eDP0_TX0- / DS10_D0-	MIP1_DSI_TX1.0_N	AE18	MIP1_DSI_TX1_D0N	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S113	eDP0_HPD / DS10_TE	DS10_TE	AB9	GPIO0_D2_d	DS10	I CMOS	1V8		Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	Runtime	
S114	LVDS1_1+ / eDP0_TX1+ / DS10_D1+	MIP1_DSI_TX1.1_P	AD17	MIP1_DSI_TX1_D1P	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S115	LVDS1_1- / eDP0_TX1- / DS10_D1-	MIP1_DSI_TX1.1_N	AC17	MIP1_DSI_TX1_D1N	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S116	LCD1_VDD_EN	LCD1_VDD_EN	AD22	GPIO0_C0_d PWM1_M0 GPUVTS UART0_RX	DS10	O CMOS	1V8		Secondary Panel Power Enable	Runtime	
S117	LVDS1_2+ / eDP0_TX2+ / DS10_D2+	MIP1_DSI_TX1.2_P	AD14	MIP1_DSI_TX1_D2P	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S118	LVDS1_2- / eDP0_TX2- / DS10_D2-	MIP1_DSI_TX1.2_N	AC14	MIP1_DSI_TX1_D2N	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S119	GND		-		PWR GND						
S120	LVDS1_3+ / eDP0_TX3+ / DS10_D3+	MIP1_DSI_TX1.3_P	AD12	MIP1_DSI_TX1_D3P	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S121	LVDS1_3- / eDP0_TX3- / DS10_D3-	MIP1_DSI_TX1.3_N	AE12	MIP1_DSI_TX1_D3N	DS10	O D-PHY			Secondary DSI Panel Differential Pair Data Lines	Runtime	
S122	LCD1_BKLT_PWM	LCD1_BKLT_PWM	AH26	GPIO0_B7_d PWM0_M0 CPUVTS	DS10	O CMOS	1V8		Secondary Panel Brightness Control	Runtime	
S123	GPIO13	NC	-		GPIO	I/O CMOS	1V8		GPIO Pin 13 Preferred Output	Runtime	
S124	GND		-		PWR GND						
S125	LVDS0_0+ / eDP0_TX0+ / DS10_D0+	MIP1_DSI_TX0_LVDS_TX0.0_P	AH17	MIP1_DSI_TX0_D0P LVDS_TX0_D0P	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S126	LVDS0_0- / eDP0_TX0- / DS10_D0-	MIP1_DSI_TX0_LVDS_TX0.0_N	AG17	MIP1_DSI_TX0_D0N LVDS_TX0_D0N	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S127	LCD0_BKLT_EN	LCD0_BKLT_EN	AD23	GPIO0_B0_d CLK32K_IN CLK32K_OUTB PCIE002_BUTTONRStn	DS10	O CMOS	1V8		Primary Panel Backlight Enable	Runtime	
S128	LVDS0_1+ / eDP0_TX1+ / DS10_D1+	MIP1_DSI_TX0_LVDS_TX0.1_P	AH16	MIP1_DSI_TX0_D1P LVDS_TX0_D1P	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S129	LVDS0_1- / eDP0_TX1- / DS10_D1-	MIP1_DSI_TX0_LVDS_TX0.1_N	AG16	MIP1_DSI_TX0_D1N LVDS_TX0_D1N	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S130	GND		-		PWR GND						
S131	LVDS0_2+ / eDP0_TX2+ / DS10_D2+	MIP1_DSI_TX0_LVDS_TX0.2_P	AH14	MIP1_DSI_TX0_D2P LVDS_TX0_D2P	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S132	LVDS0_2- / eDP0_TX2- / DS10_D2-	MIP1_DSI_TX0_LVDS_TX0.2_N	AG14	MIP1_DSI_TX0_D2N LVDS_TX0_D2N	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S133	LCD0_VDD_EN	LCD0_VDD_EN	AH25	GPIO0_C7_d HDMI_TX_CEC_M1 PWM0_M1 UART0_CTSn	DS10	O CMOS	1V8		Primary Panel Power Enable	Runtime	
S134	LVDS0_CK+ / eDP0_AUX+ / DS10_CLK+	MIP1_DSI_TX0_LVDS_TX0.4_P	AH15	MIP1_DSI_TX0_CLKP LVDS_TX0_CLKP	DS10	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S135	LVDS0_CK- / eDP0_AUX- / DS10_CLK-	MIP1_DSI_TX0_LVDS_TX0.4_N	AG15	MIP1_DSI_TX0_CLKN LVDS_TX0_CLKN	DS10	O D-PHY			Primary DSI Panel Differential Pair Clock Lines	Runtime	
S136	GND		-		PWR GND						
S137	LVDS0_3+ / eDP0_TX3+ / DS10_D3+	MIP1_DSI_TX0_LVDS_TX0.3_P	AH13	MIP1_DSI_TX0_D3P LVDS_TX0_D3P	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout
S138	LVDS0_3- / eDP0_TX3- / DS10_D3-	MIP1_DSI_TX0_LVDS_TX0.3_N	AG13	MIP1_DSI_TX0_D3N LVDS_TX0_D3N	DS10	O D-PHY			Primary DSI Panel Differential Pair Data Lines	Runtime	90 Ohm Layout

Pin #	Name STANDART	Signals_SM_RK3568	CPU PIN	CPU Function IO description Func1 Func2 Func3 Func4 Func5 Func6	Group	I/O Type	I/O Level	PU / PD SM_RK3568	Description	Power Domain	Comments
S139	I2C_LCD_CK	I2C_LCD_SCL	V5	GPIO4_B5_d I2C2_SCL_M1 EBC_S05H CAN2_TX_M0 J253_S0D3_M1	DSI	I/O OD CMOS	1V8	PU 2K2	I2C clock to read LCD display EDID EEPROMs	Runtime	
S140	I2C_LCD_DAT	I2C_LCD_SDA	V6	GPIO4_B4_d I2C2_SDA_M1 EBC_Q05P CAN2_RX_M0 ISP_FLASH_TRIGIN VOP_B1556_CLK_M1	DSI	I/O OD CMOS	1V8	PU 2K2	DDC Data Line Used for Flat Panel Detection and Control	Runtime	
S141	LCD0_BKLT_PWM	LCD0_BKLT_PWM	AE23	GPIO0_C3_d PWM4 VOP_PWM_M0 POE30X1_PERSTn_M0 MCU_JTAG_TRSTn	DSIO	O CMOS	1V8		Primary Panel Brightness Control	Runtime	
S142	GPIO12	NC	-		GPIO	I/O CMOS	1V8		GPIO Pin 12 Preferred Output	Runtime	
S143	GND	GND	-		PWR GND						
S144	eDP0_HPD / DSI0_TE	DSI0_TE	AH7	GPIO4_C4_d EDP_HPDIN_M0 GPIOF_TV_M0 SATA2_ACT_LED POE30X2_PERSTn_M2 J253_LRCK_M1	DSIO	I CMOS	1V8		Primary DSI Panel Tearing Effect Signal	Runtime	
S145	WDT_TIME_OUT#	WDT_TIME_OUT#	C23	GPIO1_D3_u FSPI_CS0n FLASH_CS0n	WATCHDOG	O CMOS	1V8		Watch-Dog-Timer Output, low active	Runtime	
S146	PCIE_WAKE#	NC	-		PCIE	I OD CMOS	3V3		PCIE wake up interrupt to host - common to PCIe links A, B, C, D	Standby	
S147	VDD_RTC	VDD_RTC	-		PWR RTC		2V...3.25V				
S148	LID#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	Standby	
S149	SLEEP#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Sleep indicator from Carrier Board. May be sourced from user Sleep button or Carrier logic. Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the Module.	Standby	
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	-		MANAGEMENT	I OD CMOS	VDD_IN	PU 10K	Power bad indication from Carrier Board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier.		
S151	CHARGING#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier during battery charging. Carrier to float the line when charge is complete.	Standby/Sleep	
S152	CHARGER_PRESNT#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Held low by Carrier if DC input for battery charger is present	Standby/Sleep	
S153	CARRIER_STBY#	CARRIER_STBY#	D23	GPIO1_D2_u FSPI_D1 FLASH_RDn	MANAGEMENT	O CMOS	1V8		The Module shall drive this signal low when the system is in a standby power state.	Standby	
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	A27	GPIO1_D4_u FSPI_D3 FLASH_CS1n	MANAGEMENT	O CMOS	1V8		Carrier Board Circuits (apart from power management and power path circuits) should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	Standby	
S155	FORCE_RECOV#	FORCE_RECOV#	B27	SARADC_VIN0	BOOT	I OD CMOS	1V8	PU 10K	Low on this pin allows nonprotected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOC's that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV pin may invoke the SOC native Force Recovery mode - such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	Standby	
S156	BATLOW#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Battery low indication to Module. Carrier to float the line in inactive state.	Standby/Sleep	
S157	TEST#	NC	-		MANAGEMENT	I OD CMOS	1V8...5V		Held Low by Carrier to Invoke Module Vendor Specific Test Functions	Standby/Sleep	
S158	GND	GND	-		PWR GND						

Ordering information

NMS-SM-RK3568- 2-16 A I 1



NMS-SM-RK3568-2-16AI1	2 GBytes LPDDR4 RAM, 16 GBytes eMMC ROM, 2 Gigabit Ethernet (GBE0, GBE1), Industrial
NMS-SM-RK3568-2-16AC1	2 GBytes LPDDR4 RAM, 16 GBytes eMMC ROM, 2 Gigabit Ethernet (GBE0, GBE1), Commercial
NMS-SM-RK3568-2-16BI1	2 GBytes LPDDR4 RAM, 16 GBytes eMMC ROM, 1 Gigabit Ethernet (GBE0), Industrial
NMS-SM-RK3568-2-16BC1	2 GBytes LPDDR4 RAM, 16 GBytes eMMC ROM, 1 Gigabit Ethernet (GBE0), Commercial